AMENDMENTS TO THE CLAIMS:

Kindly cancel claims 17-20, without prejudice. Please amend claims 1, 2, 3, 21, 22 and 23, and add new claims 24-41, as listed below.

This listing of claims will replace all prior versions and listings of claims in the Application:

Claim 1 (currently amended): A semiconductor device comprising:

a semiconductor substrate;

a gate insulation film formed on said semiconductor substrate;

a gate electrode formed on said gate insulation film and having a portion increasing upward in the length along a gate length direction, said gate electrode further having a visor portion;

a side wall formed on a side surface of said gate electrode so as to be covered behind a visor portion of said gate electrode ~~as seen in plain view~~; and

an interlayer insulation film covering said gate electrode and being in contact with said side wall,

wherein said sidewall is formed of at least two insulation films, and ~~each~~ all of said insulation films ~~contacts~~ contact both said interlayer insulation film and said gate electrode.

Claim 2 (currently amended): A semiconductor device comprising:

a semiconductor substrate;

a gate insulation film formed on said semiconductor substrate;

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a gate electrode formed on said gate insulation film and having a portion increasing upward in the length along a gate length direction, said gate electrode further having a visor portion;

a side wall formed on a side surface of said gate electrode so as to be covered behind a visor portion of said gate electrode ~~as seen in plain view~~;

an interlayer insulation film covering said gate electrode; and

a contact formed in said interlayer insulation film and being in contact with said side wall,

wherein said sidewall is formed of at least two insulation films, and ~~each~~ all of said insulation films ~~contacts~~ contact both said interlayer insulation film and said gate electrode.

Claim 3 (currently amended): A semiconductor device comprising:

a semiconductor substrate;

a gate insulation film formed on said semiconductor substrate;

a gate electrode formed on said gate insulation film and having a portion increasing upward in the length along a gate length direction, said gate electrode further having a visor portion; and

a side wall formed on a side surface of said gate electrode so as to be covered behind a visor portion of said gate electrode ~~as seen in plain view~~, said side wall being formed of a lamination of at least two insulation films having different etching properties, ~~each~~ all of said insulation films ~~contacts~~ contact both said interlayer insulation film and said gate electrode.

Claim 4 (original): The semiconductor device according to claim 1, wherein said gate electrode comprises a lower part substantially constant in the length along said gate length

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direction, and an upper part on said lower part increasing upward in the length along said gate length direction.

Claim 5 (original): The semiconductor device according to claim 2, wherein said gate electrode comprises a lower part substantially constant in the length along said gate length direction, and an upper part on said lower part increasing upward in the length along said gate length direction.

Claim 6 (original): The semiconductor device according to claim 3, wherein said gate electrode comprises a lower part substantially constant in the length along said gate length direction, and an upper part on said lower part increasing upward in the length along said gate length direction.

Cont C'

Claim 7 (previously amended): The semiconductor device according to claim 4, wherein the width of said visor portion is substantially constant and greater in length along said gate length direction than said upper or lower parts.

Claim 8 (previously amended): The semiconductor device according to claim 5, wherein the width of said visor portion is substantially constant and greater in length along said gate length direction than said upper or lower parts.

Claim 9 (previously amended): The semiconductor device according to claim 6, wherein the width of said visor portion is substantially constant and greater in length along said gate length direction than said upper or lower parts.

Claim 10 (original): The semiconductor device according to claim 2, wherein said contact reaches a diffusion layer formed at a surface of said semiconductor substrate.

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Claim 11 (previously amended): The semiconductor device according to claim 4, wherein said side wall is formed on both a side surface of said upper part and a side surface of said lower part.

Claim 12 (previously amended): The semiconductor device according to claim 5, wherein said side wall is formed on both a side surface of said upper part and a side surface of said lower part.

Claim 13 (previously amended): The semiconductor device according to claim 6, wherein said side wall is formed on both a side surface of said upper part and a side surface of said lower part.

Claim 14 (original): The semiconductor device according to claim 4, wherein a side surface of said upper part forms a tapered slope.

Claim 15 (original): The semiconductor device according to claim 5, wherein a side surface of said upper part forms a tapered slope.

Claim 16 (original): The semiconductor device according to claim 6, wherein a side surface of said upper part forms a tapered slope.

Claims 17-20 (currently cancelled)

Claim 21 (currently amended): A semiconductor device comprising:

a semiconductor substrate;

a gate insulation film formed on said semiconductor substrate;

a gate electrode formed on said gate insulation film and having a portion increasing upward in the length along a gate length direction, said gate electrode further having a visor portion;

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a side wall formed on a side surface of said gate electrode so as to be covered behind a visor portion of said gate electrode ~~as seen in plain view~~; and

an interlayer insulation film covering said gate electrode and being in contact with said side wall,

→ application: only w/ 2 ins.

wherein said ~~sidewalls are~~ sidewall is formed of at least two insulation films and every said insulation ~~films contact each other~~ film contacts every other said insulation film.

Claim 22 (currently amended): A semiconductor device comprising:

a semiconductor substrate;

a gate insulation film formed on said semiconductor substrate;

a gate electrode formed on said gate insulation film and having a portion increasing upward in the length along a gate length direction, said gate electrode further having a visor portion;

a side wall formed on a side surface of said gate electrode so as to be covered behind a visor portion of said gate electrode ~~as seen in plain view~~;

an interlayer insulation film covering said gate electrode; and

a contact formed in said interlayer insulation film and being in contact with said side wall,

wherein said ~~sidewalls are~~ sidewall is formed of at least two insulation films and every said insulation ~~films contact each other~~ film contacts every other said insulation film.

Claim 23 (currently amended): A semiconductor device comprising:

a semiconductor substrate;

a gate insulation film formed on said semiconductor substrate;

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a gate electrode formed on said gate insulation film and having a portion increasing upward in the length along a gate length direction, said gate electrode further having a visor portion; and

a side wall formed on a side surface of said gate electrode so as to be covered behind a visor portion of said gate electrode ~~as seen in plain view~~, said side wall being formed of a lamination of at least two insulation films having different etching properties, and wherein every said insulation ~~films contact each other~~ film contacts every other said insulation film.

Cont C1

Claim 24 (newly added): A semiconductor device comprising:

a semiconductor substrate;

a gate insulation film formed on said semiconductor substrate;

a gate electrode formed on said gate insulation film and having a portion increasing upward in the length along a gate length direction, said gate electrode further having a visor portion;

a side wall formed on a side surface of said gate electrode so as to be covered behind a visor portion of said gate electrode; and

an interlayer insulation film covering said gate electrode and being in contact with said side wall,

= (8b) in Fig 5, rectangular [0033]

wherein said visor portion has a three-stage structure comprising a lower part, an upper part with sides, and a visor part with sides,

said upper part is isosceles-trapezoidal in shape and shorter at the bottom;

said lower and visor parts are connected by said upper part; and

said sides of visor part and said sides of upper part form an angle of 30-60°.

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Claim 25 (newly added): A semiconductor device comprising:

a semiconductor substrate;

a gate insulation film formed on said semiconductor substrate;

a gate electrode formed on said gate insulation film and having a portion increasing upward in the length along a gate length direction, said gate electrode further having a visor portion;

a side wall formed on a side surface of said gate electrode so as to be covered behind a visor portion of said gate electrode;

an interlayer insulation film covering said gate electrode; and

a contact formed in said interlayer insulation film and being in contact with said side wall,

wherein said visor portion has a three-stage structure comprising a lower part, an upper part with sides, and a visor part with sides,

said upper part is isosceles-trapezoidal in shape and shorter at the bottom;

said lower and visor parts are connected by said upper part; and

said sides of visor part and said sides of upper part form an angle of 30≦60°.

Claim 26 (newly added): A semiconductor device comprising:

a semiconductor substrate;

a gate insulation film formed on said semiconductor substrate;

a gate electrode formed on said gate insulation film and having a portion increasing upward in the length along a gate length direction, said gate electrode further having a visor portion; and

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a side wall formed on a side surface of said gate electrode so as to be covered behind a visor portion of said gate electrode, said side wall being formed of a lamination of at least two insulation films having different etching properties,

wherein said visor portion has a three-stage structure comprising a lower part, an upper part with sides, and a visor part with sides,

said upper part is isosceles-trapezoidal in shape and shorter at the bottom;

said lower and visor parts are connected by said upper part; and

said sides of visor part and said sides of upper part form an angle of 30-60°.

cont

C1

Claim 27 (newly added): The semiconductor device according to claim 24, wherein said side wall is formed on both a side surface of said upper part and a side surface of said lower part.

Claim 28 (newly added): The semiconductor device according to claim 25, wherein said side wall is formed on both a side surface of said upper part and a side surface of said lower part.

Claim 29 (newly added): The semiconductor device according to claim 26, wherein said side wall is formed on both a side surface of said upper part and a side surface of said lower part.

Claim 30 (newly added): A semiconductor device comprising:

≡ clm 1

a semiconductor substrate;

a gate insulation film formed on said semiconductor substrate;

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a gate electrode formed on said gate insulation film and having a portion increasing upward in the length along a gate length direction, said gate electrode further having a visor portion;

a side wall formed on a side surface of said gate electrode so as to be covered behind a visor portion of said gate electrode; and

an interlayer insulation film covering said gate electrode and being in contact with said side wall,

wherein said visor portion has no overhang with respect to said side wall.

= claim 31

Claim 31 (newly added): A semiconductor device comprising:

≈ clm 2

a semiconductor substrate;

a gate insulation film formed on said semiconductor substrate;

a gate electrode formed on said gate insulation film and having a portion increasing upward in the length along a gate length direction, said gate electrode further having a visor portion;

a side wall formed on a side surface of said gate electrode so as to be covered behind a visor portion of said gate electrode;

an interlayer insulation film covering said gate electrode; and

a contact formed in said interlayer insulation film and being in contact with said side wall,

wherein said visor portion has no overhang with respect to said side wall.

Claim 32 (newly added): A semiconductor device comprising:

≈ clm 3

a semiconductor substrate;

cnt C1

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a gate insulation film formed on said semiconductor substrate;

a gate electrode formed on said gate insulation film and having a portion increasing upward in the length along a gate length direction, said gate electrode further having a visor portion; and

a side wall formed on a side surface of said gate electrode so as to be covered behind a visor portion of said gate electrode, said side wall being formed of a lamination of at least two insulation films having different etching properties, wherein said visor portion has no overhang with respect to said side wall.

cnt C1

Claim 33 (newly added): The semiconductor device according to claim 30, wherein said gate electrode comprises a lower part substantially constant in the length along said gate length direction, and an upper part on said lower part increasing upward in the length along said gate length direction. = claim 4

Claim 34 (newly added): The semiconductor device according to claim 31, wherein said gate electrode comprises a lower part substantially constant in the length along said gate length direction, and an upper part on said lower part increasing upward in the length along said gate length direction. = claim 4

Claim 35 (newly added): The semiconductor device according to claim 32, wherein said gate electrode comprises a lower part substantially constant in the length along said gate length direction, and an upper part on said lower part increasing upward in the length along said gate length direction. = claim 4

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Claim 36 (newly added): The semiconductor device according to claim 33, wherein said side wall is formed on both a side surface of said upper part and a side surface of said lower part. = claim 4

Claim 37 (newly added): The semiconductor device according to claim 34, wherein said side wall is formed on both a side surface of said upper part and a side surface of said lower part. = claim 4

cont C1

Claim 38 (newly added): The semiconductor device according to claim 35, wherein said side wall is formed on both a side surface of said upper part and a side surface of said lower part. = claim 4

Claim 39 (newly added): The semiconductor device according to claim 36, wherein a side surface of said upper part forms a tapered slope. = claim 14

Claim 40 (newly added): The semiconductor device according to claim 37, wherein a side surface of said upper part forms a tapered slope. = claim 14

Claim 41 (newly added): The semiconductor device according to claim 38, wherein a side surface of said upper part forms a tapered slope. = claim 14

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